(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER
108680

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO.
(if known, sec 37 C.F.R.1.5)
09/763365

OIPE JC47 FEB 21 2001 PATENT & TRADEMARK OFFICE

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/03968	June 16, 2000	June 23, 1999

TITLE OF INVENTION
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

APPLICANTS FOR DO/EO/US
Teruo TAKIZAWA, Hiroyuki SHIMADA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☐ Other items or information:

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/763365	INTERNATIONAL APPLICATION NO. PCT/JP00/03968	ATTORNEY'S DOCKET NUMBER 108680

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	14- 20 =	0	X $ 18.00	$	
Independent Claims	4- 3 =	1	X $ 80.00	$80.00	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$940.00	
Reduction by 1/2 for filing by small entity, if applicable. -				$	
SUBTOTAL =				$940.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$940.00	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 116431 in the amount of $940.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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09/763365
JC03 Rec'd PCT/PTO 21 FEB 2001

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Teruo TAKIZAWA, Hiroyuki SHIMADA

Application No.: U.S. National Stage
of PCT/JP00/03968

Filed: February 21, 2001 Docket No.: 108680

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claim 3 as follows:

3. (Amended) A semiconductor device according to claim 1, wherein p-type impurities are doped into said germanium film.

Please add new claim 14 as follows:

-- 14. A semiconductor device according to claim 2, wherein p-type impurities are doped into said germanium film. --

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REMARKS

Claims 1-14 are pending. By this Preliminary Amendment, claim 3 is amended and claim 14 is added to eliminate multiple dependencies. Prompt and favorable examination on the merits is respectfully solicited.

The attached Appendix includes a marked up copy of each rewritten claim (37 C.F.R. 1.121(c)(ii)).

Respectfully submitted,

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Date: February 21, 2001

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APPENDIX

Changes to Claims:

Claim 14 is added.

The following is a marked-up version of the amended claim:

3. A semiconductor device according to ~~claim 1 or 2,~~ claim 1, wherein p-type impurities are doped into said germanium film.

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Semiconductor device and manufacturing method thereof

[Field of the Invention]

The present invention relates to a semiconductor device and a manufacturing method thereof, which are favorably fitted to a metal-oxide-semiconductor field-effect transistor.

[Background of the Invention]

In a metal-oxide-semiconductor field-effect transistor (hereinafter also referred to as "MOSFET") used in a conventional semiconductor device, a polysilicon film in which impurities are deeply doped is used as a material for a gate electrode. For example, in a manufacturing process technique used in manufacturing a CMOS circuit (Complimentary MOSFET circuit), in order to balance the performance characteristic of the circuit, n-type polysilicon, in the case of n-channel MOSFET (NMOS), and p-type polysilicon, in the case of p-channel MOSFET (PMOS) are used as a material for a gate electrode. Further, for the purpose of lowering the resistance of a gate electrode, a structure to form a transition metal silicide film on the surface of the gate electrode is used.

In this case, however, the work function of an n-type polysilicon film is 4.15eV and that of a p-type polysilicon

film is 5.25eV, which results in a value largely deviating from the intrinsic mid gap energy of silicon, 4.61eV. Such large deviation of the value causes an increase in the absolute value of the flat-band voltage V_{FB} upon considering a MOS capacitor consisting of a laminated structure of a metal, an insulated film and a semiconductor (Signs are different between NMOS and PMOS). Thus, an optimum value of impurity concentration in the MOSFET channel for controlling the threshold value V_{th} is shifted close to the value of high concentration.

In such channel of high concentration, scattering by impurities has a large influence, which invites the deterioration of carrier mobility in the channel. Namely, this indicates the deterioration of the current driving ability of MOSFET and gives a material influence on the response characteristic of the circuit.

In order to solve such problem, various gate electrode materials having a work function are being suggested. "Tsu-Jae King and others" (IEDM Technical Digest 1990, page 253) and Japanese Patent Laid-Open Publication Hei 5-235335, for example, suggest a structure using an SiGe alloy film as a material for a gate electrode, and "Jeong-Mo Hwang and others" (IEDM Technical Digest 1992, page 345) suggests a structure using a TiN film.

Fig. 8 indicates the first example of related arts using an SiGe alloy film for a gate electrode. Explaining Fig. 8, it indicates a structure in which an NMOS transistor 20 and a PMOS transistor 21 are formed on a substrate 1, and an n-type polycrystalline SiGe film 30 and a p-type polycrystalline SiGe film 31 are respectively deposited on a gate oxide 2. Further, a low resistance conductive film 4 for lowering the resistance is provided on the SiGe film 30. Upon using such SiGe alloys as a gate electrode material, a work function can be shifted closer to the intrinsic mid gap energy of silicon in the proportion of germanium atoms contained in the silicon.

Further, Reference no. 5 indicates a source and drain region, Reference no. 22 an n-well region and Reference No. 23 an element separation oxide.

In the aforementioned related art example, however, a substantial improvement of characteristics can only be expected in the PMOS transistor 21. This derives from a physical phenomenon that changes in a band structure in SiGe alloy can be mainly recognized only in the valence band side. That is, the work function of the p-type polycrystalline SiGe film 31 can be controlled by mixing germanium, however, the n-type polycrystalline SiGe film 30 is no more effective

than expected.

Fig. 9 indicates an example of related arts using a TiN film for a gate electrode. In Fig. 9, the components identical to those in Fig. 8, are donated by the same reference numerals and the detailed explanation thereof is abbreviated. As in Fig. 8, Fig. 9 indicates a structure in which the NMOS transistor 20 and the PMOS transistor 21 are formed on a substrate 1, and a TiN film 32 is formed on the gate oxide 2. Further, the low resistance conductive film 4 is also provided on the TiN film 32 as provided in the first related art example.

This work function of such TiN film, as described in "Jeong Mo Hwang and others" (IEDM Technical Digest 1992, page 345), is 4.7 to 4.8eV, which is close to the intrinsic mid gap energy of silicon, 4.61eV, and is more effective.

In this case, however, as the work function of a gate electrode is uniquely determined, there is a problem that a little unbalance arises as to the characteristics of the NMOS transistor and the PMOS transistor. Further upon adopting the aforementioned low resistance conductive film 4, the dispersion in work functions is caused by a conductive film formation process, therefore, there is also a drawback that the process conditions should be strictly controlled.

[Discription of the Invention]

The present invention is made in view of the above problems, and prevents the deterioration of carrier mobility in a channel in a semiconductor, especially an NMOS transistor and a PMOS transistor, and provides a semiconductor device having a high current driving ability and a manufacturing method thereof.

In order to solve this problem, the present invention, in a metal-oxide-semiconductor field-effect transistor formed on a silicon substrate, provides a semiconductor device in which a gate electrode of such transistor is formed with a germanium film.

The germanium film can be a single-crystalline germanium film, a polycrystalline germanium film or an amorphous germanium film. Further, p-type impurities can be doped into the germanium film.

The gate electrode can comprise a multi-layer structure which includes a germanium film and a low resistance conductive film.

Further, the low resistance conductive film can include a transition metal, a transition metal silicide or

a transition metal nitride film, or a combination thereof.

Such multi-layer structure can also be provided with a polysilicon film in between a germanium film and a low resistance conductive film.

The present invention provides a semiconductor device having an n-channel metal-oxide-semiconductor field-effect transistor and a p-channel metal-oxide-semiconductor field-effect transistor which complement each other, wherein a gate electrode of each of the transistors comprises a single-crystalline germanium film, a polycrystalline germanium film or an amorphous germanium film in which p-type impurities are doped.

The present invention also provides a manufacturing method of a semiconductor device comprising a step of forming a gate oxide on a semiconductor substrate; a step of forming a germanium film on the gate oxide; a step of doping p-type impurities into the germanium fill and then patterning such germanium film to form a gate electrode; and a step of forming a source and drain region by using the gate electrode as a mask.

The step of forming the gate electrode can comprise a step of forming a polysilicon film on the germanium film,

a step of forming a transition metal on the polysilicon film and a step of annealing the polysilicon so that a part or all of such polysilicon becomes a transition metal silicide.

The step of forming the gate electrode can include a step of forming a metal transition film or a metal transition nitride film on the germanium film.

The step of doping the p-type impurities can be used by a CVD method.

Further, the step of doping the p-type impurities is used by an ion implantation method.

Furthermore, the present invention provides a manufacturing method of a semiconductor device comprising a step of forming a gate oxide on a semiconductor substrate, a step of forming a germanium film on the gate oxide, a step of doping p-type impurities into the germanium film and patterning such germanium film to form a gate electrode, a step of forming a source and drain region by using the gate electrode as a mask, a step of forming a spacer on both ends of the gate electrode, and a step of forming a transition metal film on the gate electrode and the source and drain region and a step of annealing the transition metal to form a transition metal silicide.

[Brief Explanation of the Drawings]

Fig. 1 is a sectional view showing the first embodiment of the present invention.

Fig. 2 is a diagram explaining a first manufacturing method relating to the first embodiment of the present invention.

Fig. 3 is a diagram explaining a second manufacturing method relating to the first embodiment of the present invention.

Fig. 4 is a diagram showing an energy band diagram in an MOS structure of the present invention.

Fig. 5 is a sectional view showing the second embodiment of the present invention.

Fig. 6 is a sectional view showing the third embodiment of the present invention.

Fig. 7 is a sectional view showing the fourth embodiment of the present invention.

Fig. 8 is a diagram showing an example of a related art.

Fig. 9 is a diagram showing an example of a related art.

[Preferred Embodiments of the Invention]

Next, embodiments of the present invention are explained in reference to the drawings.

The first embodiment of the present invention is shown in Fig. 1. Fig. 1 is a diagram of the case in which the present invention is applied to a p-channel MOSFET.

In a semiconductor relating to the first embodiment of the present invention, the polycrystalline germanium film 3 and the low resistance conductive film 4 are formed through the gate oxide 2 in a region of the p-type silicon substrate 1 where a gate electrode is formed. The germanium film 3 may be a single-crystalline germanium or an amorphous germanium film in addition to a polycrystalline germanium layer. A germanium film, however, has a characteristic of a p-type semiconductor by doping p-type impurities, e.g. boron (B). Further, immediately below the gate oxide 2, a channel part 6 is provided and at both ends thereof a source and drain region 5 is provided, thereby forming a MOSFET.

Thus, in this embodiment, the use of a germanium film as a gate electrode can suppress the concentration raising of impurities doped in a channel and can prevent the deterioration of carrier mobility in a channel.

Next, a manufacturing method of the present invention is explained in reference to fig. 2 and fig. 3. In the following, however, an NMOS transistor is explained, but a PMOS transistor can also be manufactured in the same way by suitably changing the impurities to be doped to the channel part 6 and the source and drain region 5.

Fig. 2 shows a first manufacturing method relating to this embodiment.

In Fig. 2(a), after borons (B^+) are first doped into a p-type silicon substrate 1 having a specific resistance of 14 to 22 Ω/cm and the surface orientation (100) to obtain a region with a low concentration of 10^{15} to 10^{17} cm^{-3} and to form the channel 6, approximately 70 to 100 angstroms of a gate electrode is formed with thermal oxidation.

Next, in Fig. 2(b), 200 to 400nm of the polycrystalline germanium film 3 is deposited by a CVD (Chemical Vapor Deposition) method and borons (B+) are doped into such film by an ion implantation method to obtain a region with a

concentration of approximately 10^{17} to $10^{20}cm^{-3}$. The details on the concentration of borons to be doped into the polycrystalline germanium film 3 at this time is described later.

Next, in Fig. 2(C), after a polysilicon film 7 is deposited on the aforementioned polycrystalline germanium film 3 by a CVD method, a transition metal film e.g. a Ti film is formed by a spattering method, and a part of the polysilicon film 7 becomes a transition metal silicide film 8 ($TiSi_2$ film) through a high temperature annealing. Further, at this time, all of the polysilicon film 7 can become a refractory silicide. Furthermore, Co, Mo, etc. can be cited as examples of transition metals, in addition to Ti.

Finally in Fig. 2(d), after applying a resist not shown in the figure and patterning a gate electrode by a photo lithography, phosphoruses (P+) are doped using this gate electrode pattern as a mask to obtain a region with a concentration of approximately $10^{20}cm^{-3}$. Consequently, the source and drain region 5 is obtained by self-alignment.

Next, a second manufacturing method relating to this embodiment is explained in reference to Fig. 3. Further, the components identical to those in Fig. 2 are donated by

the same numerals and the detailed explanation thereof are abbreviated.

First, in Fig. 3(a), as in the first manufacturing method shown in Fig. 2(a), the channel part 6 is formed on the p-type silicon substrate 1 having a specific resistance of 14 to 22 Ω/cm and the surface orientation (100), and approximately 70 to 100 angstroms of a gate electrode is formed with thermal oxidation.

Next, in Fig. 3(b), the polycrystalline germanium film 3 is deposited on the gate oxide 2 and borons (B+) are doped to become a p-type semiconductor by an ion implantation method.

Next, in Fig. 3(c), after depositing the polysilicon film 7 by a CVD method, a resist not shown in the figure is applied and a gate electrode is patterned by a photo lithography method. Using this gate electrode pattern, the source and drain region 5 is formed by self-alignment. The process of up to here is the same as that in the first manufacturing method of Fig. 2. Next, after silicon dioxide spacers 9 are formed at both ends of the gate electrode, a transition metal film, e.g. a Ti film, Co film or Mo film is formed by a spattering method and a part of the polysilicon film 7 and a surface of the source and drain region 5 becomes

the transition metal silicide film 8 through a high temperature annealing. In this manufacturing method, however, as phosphoruses (P+) are doped in the formation of the source and drain 5 into the polysilicon film 7 to form an n-type semiconductor, a p-n junction is generated between this and the polycrystalline germanium film. Accordingly, when using this second manufacturing method, in order to prevent such p-n junction from being generated, it is better that all of the polysilicon film 7 becomes a transition metal silicide.

As explained above, according to the manufacturing method in the embodiment of the present invention, it is possible to bring a work function of a gate electrode close to an intrinsic mid gap energy of silicon, therefore, the concentration raising of impurities doped in a channel can be suppressed, thereby enabling the prevention of deterioration of carrier mobility in the channel.

Here, a work function control of a gate electrode in the present invention is explained.

Fig. 4 is an energy band diagram of a MOS structure manufactured on the basis of the aforementioned first or second manufacturing method.

An electron affinity energy χ_1 of a p-type single-crystalline silicon film (channel part) is 4.05eV, an energy gap E_{g1} is 1.12eV, and the intrinsic mid gap energy is 4.61eV. Meanwhile, an electron affinity energy χ_2 is 4.0eV, an energy gap E_{g2} is 0.66eV, and an intrinsic mid gap energy E_{g2} is 4.33eV. When impurities are deeply doped into this polycrystalline germanium film to be p-type, a work function ϕ_M can be shown in the following formula (1).

$$\begin{aligned}\phi_M &= \chi_2 + Eq_2/2q + \phi_{B2} \\ &= E_{i2} + (K_BT/q)\ \mathrm{In}\ (Na/ni) \quad \cdots (1)\end{aligned}$$

Here, K_B indicates Boltzman's constant, T indicates absolute temperature, q indicates quantum of electric charge, ni indicates an intrinsic carrier concentration of germanium, and Na indicates an impurity concentration doped into a polycrystalline germanium film.

Upon bringing ϕ_M close to 4.61eV in a greenhouse (T=300K), for example, the required impurity concentration Na can be found as $1.2 \times 10^{18}\ cm^{-3}$ using the intrinsic carrier concentration of germanium of ni; $2.4 \times 10^{13}\ cm^{-3}$. At this time, the condition of an ion implantation is that the B^+ implantation energy is 50keV and the doze amount is approximately $1.0m \times 10^{13} cm^{-2}$ per a 300nm polycrystalline germanium film thickness. Further, even if the doze amount

varies within the extent of ±30%, the variation of the work function ϕ_M is no more than 0.01 V according to the formula (1), which shows the high controllability of the work function.

Further, when a material close to an intrinsic mid gap energy of Si is used as a gate electrode, an electrode of the same material can be used for an n-channel type transistor and a p-channel type transistor, but if any deviation of the work function of a Ti film ϕ_M from the intrinsic mid gap energy of Si causes a difference in a channel dope amount between the n-channel transistor and the p-channel transistor, thereby arising an unbalanced aspect in characteristic. Meanwhile, when a p-type polycrystalline germanium is used for a gate electrode, it is possible to bring such energy close to the intrinsic mid gap energy of Si by using polycrystalline germanium deeply doped to be n+ type. By this, a CMOS well-balanced in the characteristic, in which an electrode of the same material is used, can be obtained.

Regarding the doping process of p-type impurities in the first manufacturing method and the second manufacturing method relating to the first embodiment of the present invention, only those by an ion implantation method is mainly explained in the above, but in place of such ion implantation

method, the p-type polycrystalline germanium film 3 may also be formed by a CVD method using a mixed gas of GeH_4 and B_2H_6. This case brings an advantage that an ion plantation process and an impurity thermal diffusion process required subsequent to such ion implantation process can be omitted.

Next, the second embodiment of the present invention is explained in reference to Fig. 5. Further, the components identical to those in the aforementioned first embodiment are donated by the same numerals.

In a semiconductor device relating to the second embodiment of the present invention, the polycrystalline germanium film 3 is formed through the gate oxide 2 in the region of the p-type silicon substrate 1 where a gate electrode is formed. On the p-type polycrystalline germanium film 3, a transition metal film 10 is directly formed as a low resistance conductive film by a spattering method. For this transition metal, Mo, etc., which is chemically stable and has a lower specific resistance among the transition metals, is desirable. Thus, in the case of directly forming a transition metal on the p-type polycrystalline germanium film 3, high temperature annealing is not required. Therefore, this solves a problem that the impurities doped on the p-type polycrystalline germanium film 3 are penetrated into the gate oxide 2.

Especially in a very thin gate oxide (no more than 3nm), this embodiment can be an effective means. Further, Reference no. 5 indicates a source and drain region and Reference no. 6 indicates a channel part.

Next, the third embodiment of the present invention is explained in reference to Fig. 6. Further, the components identical to those in the aforementioned conventional example of Fig. 8 are donated by the same numerals.

Fig. 6 indicates a structure in which the PMOS transistor 21 and the NMOS transistor 20 are formed on the p-type silicon substrate 1, and in the region of the PMOS transistor 21 on the p-type silicon substrate 1, an n-well region 22 is formed and is separated from the NMOS transistor 20 through an element separation oxide 23. In both the NMOS transistor and the PMOS transistor, 200 to 400nm of the polycrystalline germanium film 3 is deposited on the gate insulation film 2 by a CVD (Chemical Vapor Deposition) method, and borons (B^+) are deeply doped into such films by an ion implantation method to obtain a region with a concentration of approximately 10^{17} to $10^{20}cm^{-3}$. By this, the work function of the p-type polycrystalline germanium film 3 is brought close to the intrinsic mid gap energy. Accordingly, no difference arises as to the concentration of the impurities

doped in the channel parts of the NMOS and the PMOS, therefore, a well-balanced CMOS characteristic is obtained. Further, Reference no. 4 indicates a low resistance conductive film, Reference no. 5 a source and drain region and Reference no. 6 a channel part.

Next, the fourth embodiment of the present invention is explained using Fig. 7.

In a semiconductor relating to the fourth embodiment, an insulation film 24 is provided on the p-type silicon substrate 1, and the NMOS transistor 20 and the PMOS transistor 21, which have the same structures as those in the second embodiment shown in Fig. 5, are formed on the insulation film 24. In this embodiment, the work function of the p-type polycrystalline germanium film 3 is also brought close to the intrinsic mid gap energy of silicon. Accordingly, no difference arises as to the concentration of the impurities doped in the channel parts of the NMOS and the PMOS, therefore, a well-balanced CMOS characteristic is obtained.

MOSFET, generally referred to as Silicon on Insulator (SOI) MOSFET, is a device structure favorable for speeding up and lowering electric power consumption. For the insulation film 24, an embedded oxide (silicon dioxide) is

often used, and for an embedding technique, techniques of implanting an oxygen ion and of bonding a wafer, on which a thermal oxide is formed, on another wafer, etc. are generally adopted. In this MOSFET case, as a silicon film (SOI film) to be a channel part is formed with a thin film, in order to maintain a threshold value equivalent to a bulk MOSFET, impurities of higher concentration should be doped into such thin film. This may cause the deterioration of carrier mobility. Therefore, compensating this deterioration by controlling the work function in accordance with the present invention, and suppressing the concentration of the impurities to be doped into the channel will be highly effective means for improving carrier mobility.

According to the present invention, as the work function of a gate electrode can be well-controllably brought close to the intrinsic mid gap energy of silicon, it is possible, whether an NMOS transistor or PMOS transistor, to lower the concentration of impurities in a channel. Therefore, the deterioration of the carrier mobility can be prevented and a MOSFET having a high current driving ability can be provided.

What is claimed is:

1. A semiconductor device comprising:

a silicon substrate and

a metal-oxide-semiconductor field-effect transistor formed on said silicon substrate,

wherein a gate electrode of said transistor comprises a germanium film.

2. A semiconductor device according to claim 1, wherein said germanium film comprises any one of a single-crystalline germanium film, a polycrystalline germanium film or an amorphous germanium film.

3. A semiconductor device according to claim 1 or 2, wherein p-type impurities are doped into said germanium film.

4. A semiconductor device according to claim 1, wherein said gate electrode comprises a multi-layer structure that includes a low resistance conductive film.

5. A semiconductor device according to claim 4, wherein said low resistance conductive film comprises a transition metal, a transition metal silicide, or a transition metal nitride film, or a combination thereof.

6. A semiconductor device according to claim 4, wherein said multi-layer structure is provided with a polysilicon film in between said germanium film and said low resistance conductive film.

7. A semiconductor device comprising:

an n-channel metal-oxide-semiconductor field-effect transistor and

a p-channel metal-oxide-semiconductor field-effect transistor,

wherein a gate electrode of each of said transistors comprises any one of a single-crystalline germanium film, a polycrystalline germanium film or an amorphous germanium film in which p-type impurities are doped.

8. A manufacturing method of a semiconductor device comprising:

a step of forming a gate oxide on a semiconductor substrate;

a step of forming a germanium film on said gate oxide;

a step of doping p-type impurities into said germanium film and patterning said germanium film to form a gate electrode; and

a step of forming a source region and a drain region by using said gate electrode as a mask.

9. A manufacturing method of a semiconductor device according to claim 8, wherein the step of forming said gate electrode comprises:

a step of forming a polysilicon on said germanium film;

a step of forming a transition metal on said polysilicon film; and

a step of annealing said polysilicon so that a part or all of said polysilicon becomes a transition metal silicide.

10. A manufacturing method of a semiconductor device according to claim 8, wherein the step of forming said gate electrode includes a step of forming a metal transition film or a metal transition nitride film on said germanium film.

11. A manufacturing method of a semiconductor device according to claim 8, wherein said p-type impurities are doped by a CVD method.

12. A manufacturing method of a semiconductor device according to claim 8, wherein said p-type impurities are doped by an ion implantation method.

13. A manufacturing method of a semiconductor device comprising:

a step of forming a gate oxide on a substrate of a semiconductor substrate;

a step of forming a germanium film on said gate oxide;

a step of doping p-type impurities into said germanium film and patterning said germanium film to form a gate electrode;

a step of forming a source region and a drain region by using said gate electrode as a mask;

a step of forming a spacer on both ends of said gate electrode; and

a step of forming a transition metal film on said gate electrode and said source region and a drain region and annealing said transition metal film to form.

Abstract

A semiconductor device comprising a metal-oxide-semiconductor field-effect transistor well controllably brings the work function of a gate electrode close to the intrinsic mid gap energy of silicon, thereby lowering the concentration of impurities in a channel. By this, the deterioration of carrier mobility is prevented and a metal-oxide-semiconductor field-effect transistor is obtained. A gate electrode has a multi-layer structure of a p-type polycrystalline or a single-crystalline germanium film 3 and a low resistance conductive film 4.

FIG.1

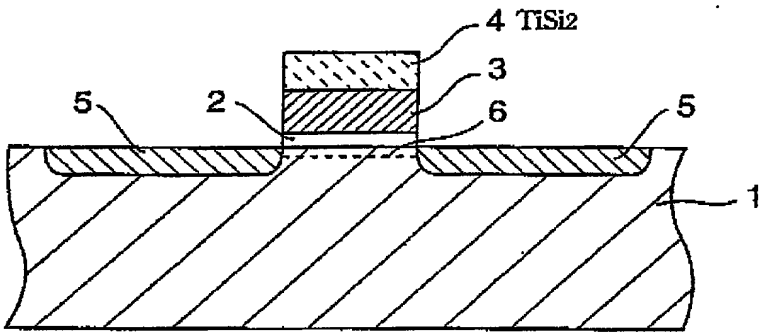

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FIG.2

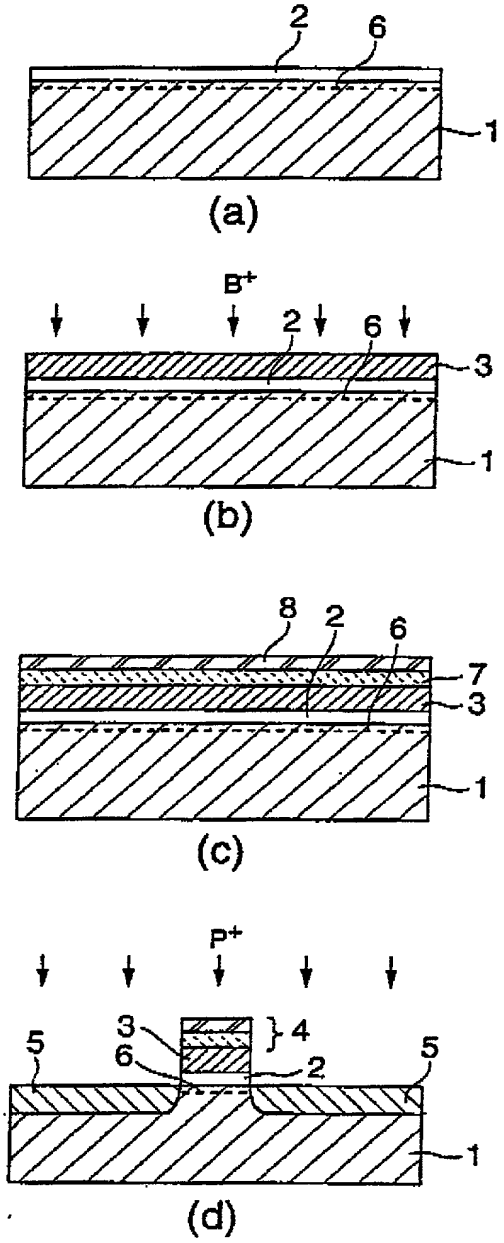


FIG.3

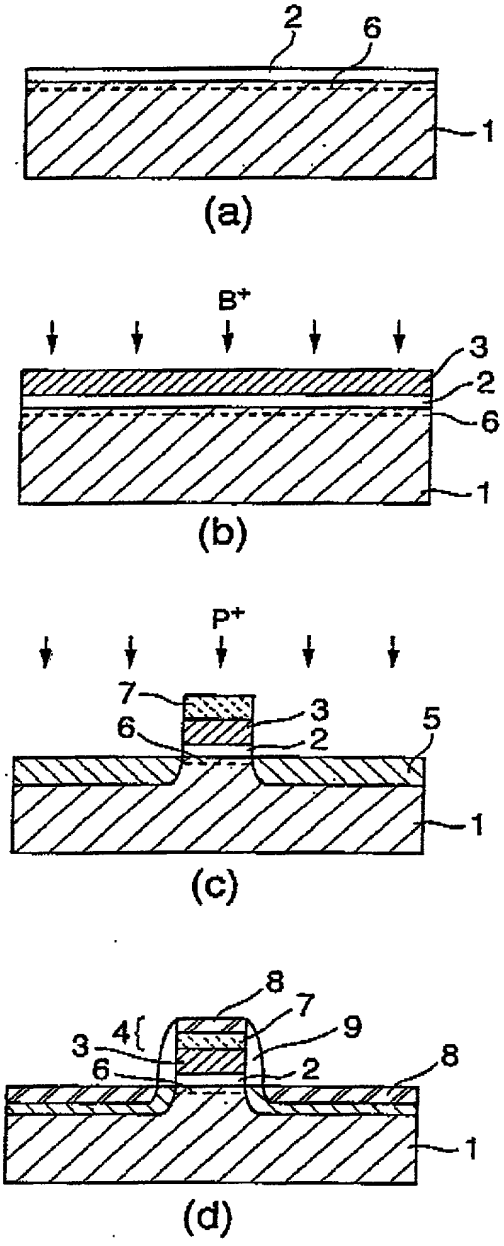
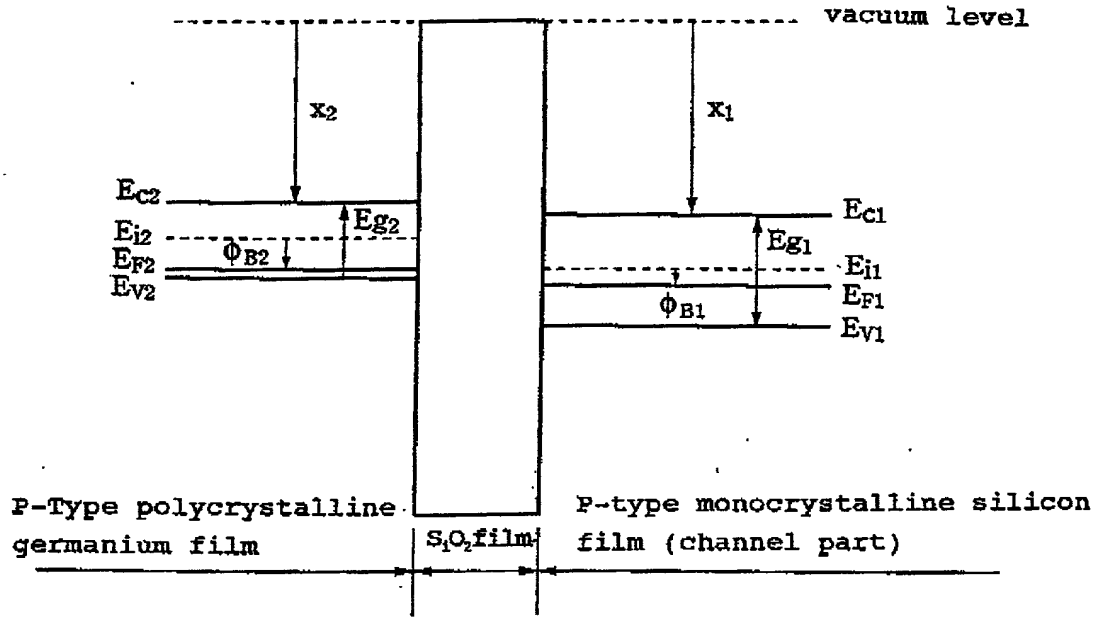


FIG. 4



E_C : conduction band edge
E_V : valence band edge
E_F : Fermi energy
E_i : intrinsic mid gap energy
x : electron affinity energy
Eg : energy gap
ϕ_B : $E_F - E_i$

FIG.5

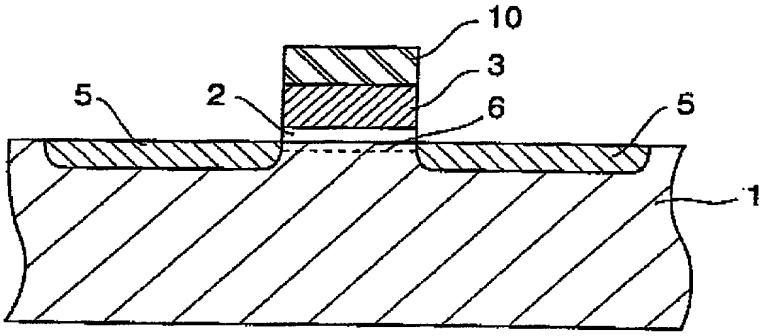


FIG.6

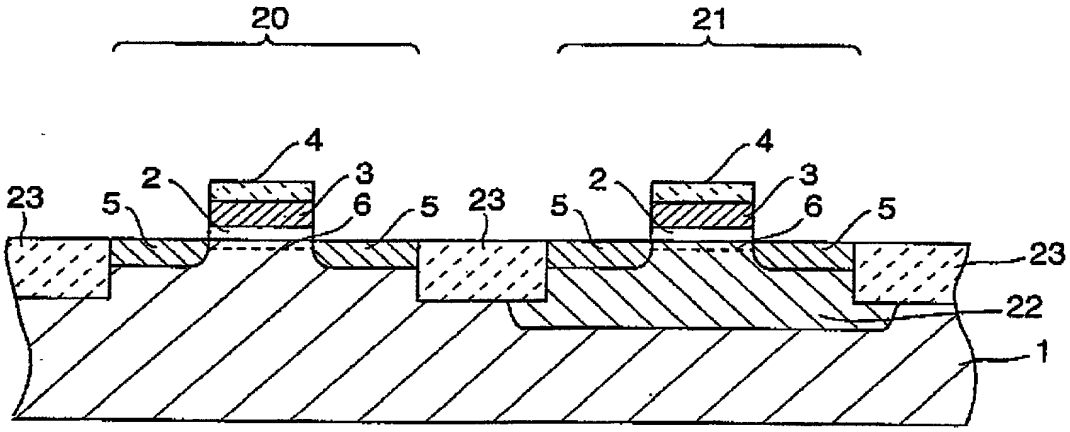


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FIG.7

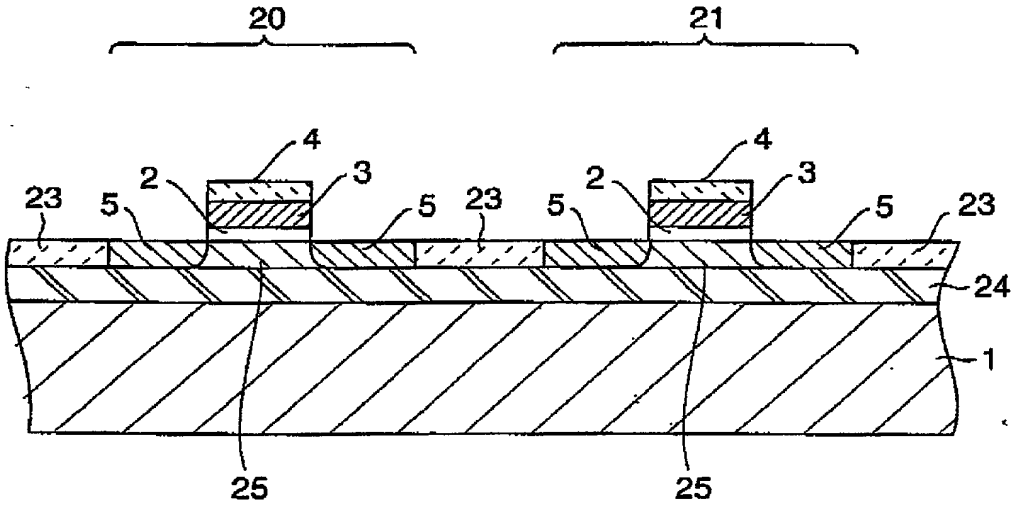

FIG.8

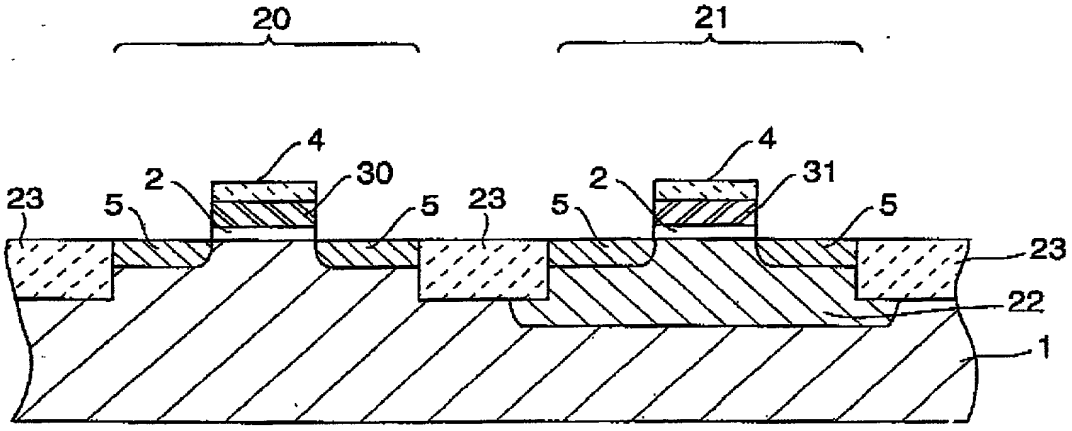

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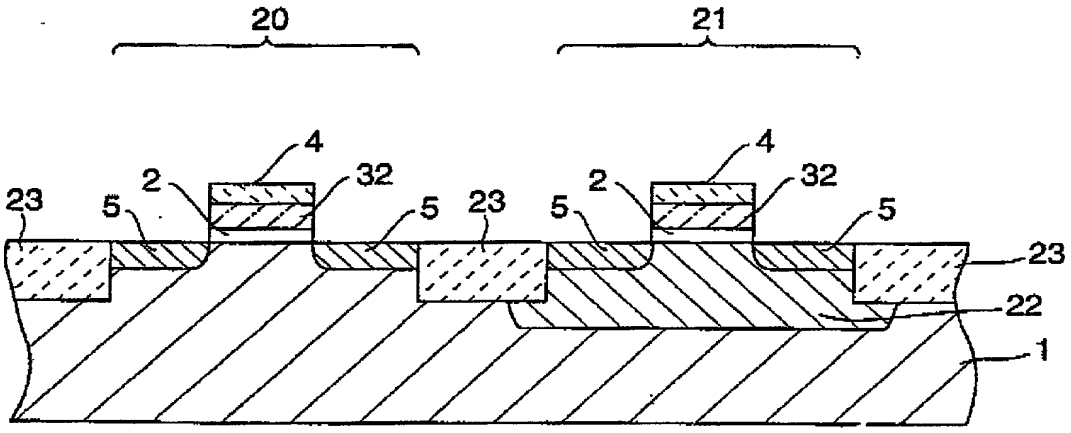
FIG.9



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特許出願宣言書及び委任状

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日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。	As a below named inventor, I hereby declare that:
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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
11-177078(P) (Number) (番号)	Japan (Country) (国名)	23/June/1999 (Day/Month/Year Filed) (出願年月日)	☐
			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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PCT/JP00/03968 (Application No.) (出願番号)	16/June/2000 (Filing Date) (出願日)	Pending (Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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Edward P. Walker, (Reg. 31,450)
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Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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(Supply similar information and signature for third and subsequent joint inventors.)